High Performance Narrow-Band Transceiver IC

Silicon Anomaly Sheet

ADF7021

This anomaly sheet describes the known bugs, anomalies, and workarounds for the ADF7021 narrow-band transceiver. This relates to Silicon Revision 4, which has a corresponding silicon revision readback code of 0x2104. See the ADF7021 data sheet for details on how to perform a silicon revision readback.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices works to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADF7021 SILICON REVISION HISTORY

Silicon Revision Readback	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
0x2104	ADF7021BCPZ	Release	Rev. A	4

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ANOMALIES

1. Sync Word Detect (SWD) Bug In 4FSK Mode [er001]:

Background:	The sync word detect (SWD) is an interrupt signal provided by the ADF7021 upon reception of a certain bit sequence. It can be used to indicate to the host microcontroller that a valid packet is being received.
Issue:	It is not possible to access the sync word detect signal on the SWD pin (Pin 33) in 4FSK mode. This is because the test DAC output is automatically muxed to the SWD pin in 4FSK mode.
Workaround:	The sync word detect function can be performed in a microcontroller by monitoring the incoming receive data (from the TxRxDATA pin) and checking against the wanted sync byte or start-of-frame delimiter. The sync word detect feature is not affected in either 2FSK or 3FSK modes.
Related Issues:	None.

2. Using IF Filter Fine Calibration for TCXO/Crystal Values Above 16.7 MHz [er002]:

Background:	The ADF7021 has selectable IF filter bandwidth settings of 25 kHz, 18.75 kHz, and 12.5 kHz, which act to perform channel selection and reject out-of-band signals. The IF filter is implemented in the analog domain and is a fifth-order Butterworth polyphase design centered at the IF of 100 kHz. To compensate for manufacturing tolerances, the IF filter should be calibrated after power-up to ensure that the bandwidth and center frequency are correct. Coarse calibration and fine calibration schemes are provided to offer a choice between fast calibration with the coarse calibration and high filter centering accuracy with fine calibration.
Issue:	The ADF7021 data sheet recommends placing the lower and upper fine calibration tones at 65.8 kHz and 131.5 kHz, respectively, by using the following formulas (see the ADF7021 data sheet for further details on Register 6, the IF fine calibration setup register): $\frac{XTAL}{IF\_CAL\_LOWER\_TONE\_DIVIDE \times 2} = 65.8\ \text{kHz}$ $\frac{XTAL}{IF\_CAL\_UPPER\_TONE\_DIVIDE \times 2} = 131.5\ \text{kHz}$ However, this is not possible for a crystal or TCXO value above 16.7 MHz because of the resolution provided in the IF fine calibration setup register.
Workaround:	Users should first check to see if a fine calibration is required for their setup. Refer to the ADF7021 data sheet on IF filter calibration for details. If a fine filter calibration is required, any one of the three workarounds listed in Table 1 can be used.
Related Issues:	None.

Table 1. Workarounds for Fine Filter Calibration

Workaround	Description
1	Use an XTAL or a TCXO value below 16.7 MHz.
2	For applications requiring an XTAL or a TCXO value above 16.7 MHz and less than 21.33 MHz, perform the sequence listed in Table 2. This programming sequence should be inserted in the receiver power-up sequence after the Register 3 write, which replaces the normal fine IF filter calibration register writes to Register 6 and Register 5. Refer to the ADF7021 data sheet for the standard receiver power-up sequence.
3	There is no fine IF filter calibration workaround in place for XTAL or TCXO values > 21.33 MHz. In this case, users are recommended to perform a coarse IF filter calibration only.

Table 2. Register Programming Sequence for IF Filter Fine Calibration Workaround

Sequence Number	Register Number	Register Write	Description
1	15	0xC000 000F	Override the IF filter gain and bandwidth setting for the IF filter calibration routine.
2	4	0xXXXX XXX4	Set the IF filter bandwidth to 18.75 kHz. Keep all other Register 4 settings as recommended in the data sheet.
3	9	0x0004 0009	Set the IF filter gain to low and AGC to manual mode.
4	6	0xXXXX XXX6	Set the IF_FINE_CAL bit. Set the IF_CAL_DWELL_TIME bits as recommended in the ADF7021 data sheet. Place the lower and upper tones at 84 kHz and 114.7 kHz, respectively, using the formulas for the fine calibration filter tones in the data sheet.
5	5	0xXXXX XXX5	Set the IF_CAL_COARSE bit. This performs a coarse calibration immediately, followed by a fine calibration. Wait until the filter calibration (coarse plus fine) is complete. This typically takes 5.2 ms. Alternatively, users can monitor the FILTER_CAL_COMPLETE signal to ascertain when the filter calibration routine is complete. This signal is programmed to appear on MUXOUT using Register 0.
6	9	0x0002 31E9	Set the AGC to automatic gain control. This should be done only after the IF filter calibration routine is complete.
7	15	0x0000 000F	Reset the test mode register (Register 15).

3. Using IF Filter Coarse Calibration for TCXO or Crystal Values Above 25.55 MHz [er003]:

Background: The IF filter coarse calibration requires that the IF filter clock (set by the IF_FILTER_DIVIDER bits (R5_DB[5:13])) is 50 kHz, according to:

$$\frac{XTAL[Hz]}{IF\_FILTER\_DIVIDER} = 50\ \text{kHz}$$

Issue: The maximum value of IF_FILTER_DIVIDER is 511, which only allows a maximum XTAL or TCXO value of 25.55 MHz. Using a frequency between 25.55 MHz and 26 MHz gives an IF filter clock greater than 50 kHz, which results in the IF filter being not centered after a coarse calibration.

Workaround: There are three possible workarounds; see Table 3.

Related Issues: None.

Table 3. Workarounds for Coarse Filter Calibration

Workaround	Description
1	Use a XTAL or TCXO value of 25.55 MHz or less.
2	Perform a fine calibration of the IF filter to account for the adjustment error introduced by the coarse calibration. This centers the IF filter within the accuracy specified by the fine calibration in the ADF7021 data sheet. Note that there is an errata related to the fine calibration of the IF filter, which is also described in this anomaly sheet.
3	If the user wishes to perform a coarse calibration only, then it is possible to manually adjust the IF filter after the coarse calibration to account for the offset introduced by the IF filter clock being greater than 50 kHz. The manual adjust is performed by programming the IF_FILTER_ADJUST bits in Register 5. The value to program depends on the XTAL or TCXO frequency being used. The calibration enable (IF_CAL_COARSE = 1) and the adjustment value (IF_FILTER_ADJUST = adjustment setting) can be written to the ADF7021 in the same single register write. This performs a coarse calibration followed by the adjustment.

4. Performing Readback During Packet Reception [er004]

Background:	An internal timing issue can result in bit errors when performing a readback from the ADF7021 during packet reception. The timing issue is related to the CDR clock and the SCLK.
Issue:	If the SCLK edge rises in a 5 ns window before the CDR clock edge, then the envelope detector circuit of the ADF7021 may experience a reset of its threshold. This results in bit errors if the AFC or linear demodulator is being used for demodulation because both these circuits use the envelope detector. If the correlator demodulator is being used without AFC, then this issue is not present.
Workaround:	There are three possible workarounds; see Table 4.
Related Issues:	None

Table 4. Workarounds for Readback During Packet Reception

Workaround	Description
1	Ensure that a readback is not performed during packet reception.
2	Ensure that the SCLK edge does not rise in a 5 ns window before the CDR positive clock edge. The CDR clock signal is available via the CLKOUT pin using the CLK_MUX test modes (R15_DB[17:19]).
3	Use the lock threshold mode (LOCK_THRESHOLD_MODE (R12_DB[4:5])) for packet reception. This locks the threshold of the envelope detector (as well as the AFC and AGC circuits). It can be set to lock on reception of a valid SWD (LOCK_THRESHOLD_MODE = 1 or LOCK_THRESHOLD_MODE = 2) or manually set at any time (LOCK_THRESHOLD_MODE = 3). Once the threshold has locked, a readback can be performed without any bit errors.

AD7021 ANOMALIES STATUS

Reference Number	Description	Status
er001	Sync word detect (SWD) bug in 4FSK mode	Refer to the workaround described in the Anomalies Section
er002	Using IF filter fine calibration for TCXO/crystal values above 16.7 MHz	Refer to the workaround described in the Anomalies Section
er003	Using IF filter coarse calibration for TCXO or crystal values above 25.55 MHz	Refer to the workaround described in the Anomalies Section
er004	Performing readback during packet reception	Refer to the workaround described in the Anomalies Section